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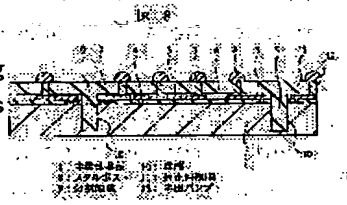
(54) METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To enhance reliability of electrical connection between a semiconductor device and a resin printed board by relaxing strain between them.
SOLUTION: Major surface of a semiconductor substrate 1 is coated with sealing resin 11 including the interior of grooves 10 and solder bumps 12 are formed on the upper surface of metal posts 8. Subsequently, the semiconductor substrate 1 and the sealing resin 11 are diced along dividing regions 9 to produce individual semiconductor devices where the major surface and the side faces of the semiconductor substrate 1 are covered with the sealing resin 11. According to the method, difference in the coefficient of thermal expansion can be reduced between the semiconductor device and the resin printed board.



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CLAIMS

[Claim(s)]
[Claim 1] (a) It is the semi-conductor wafer which has two or more chip formation fields divided by the division field. The process for which the semi-conductor wafer with which each of two or more of said chip formation fields has two or more semiconductor devices and two or more bonding pads is prepared, (b) — the conductor electrically connected to two or more bonding pads of each of said chip formation field — the process which forms the section — (c) by cutting the process which forms a slot in said division field, the process which forms the insulator layer for the closures on the principal plane of said semi-conductor wafer including the inside of the (d) aforementioned slot, and the (e) aforementioned semi-conductor wafer along said slot said conductor — the manufacture approach of the semiconductor device characterized by including the process which forms two or more semiconductor chips with which the section was formed and said a part of insulator layer for the closures was formed in the side face.
[Claim 2] (a) It is the semi-conductor wafer which has two or more chip formation fields divided by the division field. The process for which the semi-conductor wafer with which each of two or more of said chip formation fields has two or more semiconductor devices and two or more bonding pads is prepared, (b) — the conductor electrically connected to two or more bonding pads of each of said chip formation field — the process which forms the section — (c) The process which forms a slot in said division field, the process which forms the insulator layer for the closures on the principal plane of said semi-conductor wafer including the inside of the (d) aforementioned slot, (e) by grinding the rear face of said semi-conductor wafer, and cutting the process and the (f) aforementioned semi-conductor wafer which expose the insulator layer for the closures formed in said slot at the rear face of said semi-conductor wafer from the base of said slot along said slot said conductor — the manufacture approach of the semiconductor device characterized by including the process which forms two or more semiconductor chips with which the section was formed and said a part of insulator layer for the closures was formed in the side face.
[Claim 3] The manufacture approach of the semiconductor device characterized by including the process which is the manufacture approach of a semiconductor device according to claim 1 or 2, and connects a solder bump to the terminal location on the principal plane of said semi-conductor wafer electrically before forming said two or more semiconductor chips.
[Claim 4] The semiconductor device characterized by having the structure with which it is the semiconductor device with which two or more semiconductor devices were formed on the principal plane of a semiconductor chip, and the top face and side face of said semiconductor chip are covered by the insulator layer for the closures, and which the base of said semiconductor chip exposes to an inferior surface of tongue.
[Claim 5] The semiconductor device which is a semiconductor device according to claim 4, and is characterized by having the structure where some or the whole surface of a side face of said semiconductor chip was covered by the insulator layer for the closures.
[Claim 6] It is the semiconductor device characterized by being a semiconductor device according to

claim 4 or 5, and said semiconductor chip having the structure where the inferior surface of tongue was ground after being covered by the insulator layer for the closures.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] About the manufacture approach of a semiconductor device, and a semiconductor device technique, especially this invention is applied to the packaging technique of a semiconductor device, and relates to an effective technique.
[0002]
[Description of the Prior Art] Thin-shape-izing, and small and lightweight-izing are called for also about the package of a semiconductor device with small and lightweight-izing of electronic equipment. CSP (Chip Size Package) is the generic name of a package equivalent to the size of a semiconductor chip, or slightly large, and when small and lightweight-ization are realizable, since an internal wire length can be shortened, it is put in practical use as package structure where signal delay, a noise, etc. can be reduced. Although there are various the manufacture approaches of CSP, after cutting down a semiconductor chip from a semi-conductor wafer, it is common that carry the semiconductor chip on a wiring substrate equivalent to a semiconductor chip or slightly big, and it carries out a resin seal in the condition.
[0003] On the other hand, there is a wafer process package (it abbreviates to WPP below Wafer Process Package;) technique as such other manufacturing technologies of CSP. After two or more semiconductor chips formed in the semi-conductor wafer through the wafer process are put in block with the condition of a semi-conductor wafer and this technique carries out a resin seal, it is a technique which cuts down each semiconductor device from that semi-conductor wafer. In this technique, a production process can be simplified, a manufacturing cost can be reduced and there is the outstanding description that CSP can be miniaturized sharply, further.
[0004] in addition, about this kind of technique, Nikkei Business Publications, February 1, 1999 issue, and "Nikkei micro device February, 1999 issue" p 56 have a publication, for example, the manufacturing technology of CSP which perform assembly of a package in a wafer process be indicate, and where each semiconductor device be cut down from a semi-conductor wafer, that cross section have structure to which the resin for the closures lapped on the principal plane of a semiconductor chip.
[0005]
[Problem(s) to be Solved by the Invention] However, in this WPP, since each semiconductor chip is cut down from that semi-conductor wafer after carrying out the resin seal of two or more semiconductor chips of a semi-conductor wafer collectively, the resin seal of the side face and rear face of a semiconductor chip is not carried out. For this reason, the technical problem from which improvement in

package properties, such as the moisture resistance of a semiconductor device and protection-from-light nature, is prevented occurs. Moreover, only for the structure where the resin for the closures has lapped on the principal plane of a semiconductor chip, the adhesive property of said semiconductor chip and said resin for the closures may worsen, and it may exfoliate by the curve of said semiconductor chip etc., and destruction of the solder connection to the exterior of said semiconductor chip occurs, or the dependability of a resin seal falls.

[0006] Furthermore, in this WPP, compared with a semiconductor chip, since the thickness of the resin for the closures is thin, it will depend for the mechanical characteristics of a semiconductor device on a semiconductor chip. Therefore, since distortion resulting from the difference of the coefficient of thermal expansion of the substrate made of resin, such as glass epoxy of the exterior of said semiconductor device, and said semiconductor device cannot be eased, the mechanical reliability of the solder of the external connection of said semiconductor device falls.

[0007] The purpose of this invention is to offer the technique which can raise the humidity-tolerant reliability of the package of a semiconductor device, and the reinforcement effectiveness of the post for connection to the exterior.

[0008] Moreover, other purposes of this invention are to offer the technique which raises the electrical installation nature of said semiconductor device and external substrate.

[0009] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.

[0010]

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.

[0011] (1) After two or more semiconductor chips formed in the semi-conductor wafer through the wafer process are put in block with the condition of a semi-conductor wafer and the semiconductor device of this invention carries out a resin seal, it is a semiconductor device cut down from the semi-conductor wafer, and covers some or the whole surface of a side face of a semi-conductor substrate with the resin for the closures.

[0012] (2) A semiconductor device is formed in the principal plane of a semi-conductor substrate, the semiconductor device of this invention covers the principal plane and the side face of said semi-conductor substrate with the resin for the closures, and a semi-conductor substrate exposes a rear face.

[0013] (3) After the semiconductor device of this invention covers the principal plane of a semi-conductor substrate, and the side face of said semi-conductor substrate with the resin for the closures, it grinds the rear face of said semi-conductor substrate, and serves as a configuration which carried out the resin seal of the whole surface of the side face of said semi-conductor substrate.

[0014] (4) The manufacture approach of the semiconductor device of this invention includes the following processes.

[0015] (a) It is the semi-conductor wafer which has two or more chip formation fields divided by the division field. The process for which the semi-conductor wafer with which each of two or more of said chip formation fields has two or more semiconductor devices and two or more bonding pads is prepared, (b) — the conductor electrically connected to two or more bonding pads of each of said chip formation field — the process which forms the section — (c) by cutting the process which forms a slot in said division field, the process which forms the insulator layer for the closures on the principal plane of said semi-conductor wafer including the inside of the (d) aforementioned slot, and the (e) aforementioned semi-conductor wafer along said slot said conductor — the process which forms two or more semiconductor chips with which the section was formed and said a part of insulator layer for the closures was formed in the side face.

[0016] (5) The manufacture approach of the semiconductor device of this invention includes the

following processes.
[0017] (a) It is the semi-conductor wafer which has two or more chip formation fields divided by the division field. The process for which the semi-conductor wafer with which each of two or more of said chip formation fields has two or more semiconductor devices and two or more bonding pads is prepared, (b) — the conductor electrically connected to two or more bonding pads of each of said chip formation field — the process which forms the section — (c) The process which forms a slot in said division field, the process which forms the insulator layer for the closures on the principal plane of said semi-conductor wafer including the inside of the (d) aforementioned slot, (e) by grinding the rear face of said semi-conductor wafer, and cutting the process and the (f) aforementioned semi-conductor wafer which expose the insulator layer for the closures formed in said slot at the rear face of said semi-conductor wafer from the base of said slot along said slot said conductor — the process which forms two or more semiconductor chips with which the section was formed and said a part of insulator layer for the closures was formed in the side face.
[0018] According to the process of the above (4) and (5), for a wrap reason, the adhesive strength of the resin for the closures and a semi-conductor substrate becomes [the resin for the closures] strong about the principal plane and side face of a semi-conductor substrate. Therefore, exfoliation of the resin for the closures and a semi-conductor substrate can be prevented, for example, reinforcement of the post the improvement in the humidity-tolerant reliability of a semi-conductor substrate and for connection with the exterior can be performed.
[0019] Furthermore, adhesion with a semi-conductor substrate is held by the good resin for the closures, since the mechanical property of a semiconductor device is close to said resin for the closures, between the resin printed circuit boards in which said semiconductor device and said semiconductor device are mounted, the post for connection with said exterior eases distortion by the difference of a coefficient of thermal expansion, and it can improve the dependability of electrical installation.
[0020] Moreover, according to the process of (5), the side face of a semi-conductor substrate is completely covered by the resin for the closures, and since it is reinforced, the mechanical strength of a semiconductor device becomes strong. Therefore, it becomes possible in the state of the semi-conductor wafer before cutting said semi-conductor substrate and dividing into each semiconductor chip to form a solder bump, and the productive efficiency of CSP of thin wafer level can be improved.
[0021]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail based on a drawing. In addition, in the complete diagram for explaining the gestalt of operation, the same sign is given to the member which has the same function, and explanation of the repeat is omitted.
[0022] (Gestalt 1 of operation) In the gestalt 1 of this operation, the case where it applies to the manufacture approach of the semiconductor device of the CSP mold used for DRAM (Dynamic Random Access Memory) and SRAM (Static RandomAccess Memory) in which the electronic instrument of small and pocket molds, such as an information processor of a cellular phone, a pocket mold personal computer, or a pocket mold, has this invention, or a microcomputer is explained.
[0023] the sectional view having shown an example of a semiconductor device by which drawing 1 (a) is manufactured according to the gestalt 1 of this operation — it is — (b) —a part of the semiconductor device — it is a fracture perspective view.
[0024] The semi-conductor substrate 1 is the semiconductor chip which formed the semi-conductor wafer with which it consisted of a silicon single crystal, and two or more semiconductor device and two or more wiring layers 2, such as MISFET (Metal Insulator Semiconductor Field Effect Transistor), were formed on the principal plane by cutting in a division field.
[0025] A wiring layer 2 consists of an aluminum and aluminum-copper alloy or an aluminum-silicon-copper alloy. This wiring layer 2 is protected by the insulator layer 3.
[0026] An insulator layer 3 consists of the organic film, a silicon nitride film, or silicon oxide film, such as

polyimide. Opening 4 is formed in said insulator layer 3, and the wiring layer 2 and the wiring layer 5 of each other formed in the top face of an insulator layer 3 are electrically connected to it through this opening 4. A wiring layer 5 consists of copper or a copper alloy.

[0027] A wiring layer 5 is wiring for relocation of a bonding pad, and it is used in order to make a connection terminal location with the exterior the metal post 8. The front face of this wiring layer 5 is covered with the surface protective coat 6 which consists of organic film, such as polyimide. It becomes possible to raise the stopping-power force of alpha rays in this case.

[0028] a part of surface protective coat 6 — a part of wiring layer 5 — ****** — the opening [like] 7 is formed and the wiring part exposed from this opening 7 forms a bonding pad. This bonding pad is an electrode which pulls out outside electrodes formed in said semiconductor chip, such as said semiconductor device, circuit, etc. Moreover, the solder bump 12 is electrically connected to this bonding pad through the metal post 8. The metal post 8 consists of copper. The solder bump 12 consists of gold or lead-tin alloy solder.

[0029] The resin 11 for the closures (insulator layer for the closures) has also covered the side-attachment-wall section of said semi-conductor substrate 1, bites as the semi-conductor substrate 1, and is excellent in an adhesive property with said semi-conductor substrate 1 with an anchor effect. For this reason, while the humidity-tolerant reliability of said semi-conductor substrate 1 and a wiring layer 2 improves, the reinforcement effectiveness of the metal post 8 increases. This resin 11 for the closures consists of resin of an epoxy system.

[0030] Drawing 2 is the sectional view showing an example in the condition that the semiconductor device manufactured according to the gestalt 1 of this operation was mounted in the resin printed circuit board 13. Adhesion with the semi-conductor substrate 1 is held by the good resin 11 for the closures, and since the mechanical property of said semiconductor device is close to said resin 11 for the closures and the metal post 8 can control distortion of the solder bump 12 even when distortion by the difference of a coefficient of thermal expansion occurs between said semiconductor device and the resin printed circuit board 13 which has the connection pad 14, it can improve the dependability of electrical installation.

[0031] Next, according to drawing 3 - drawing 8 , the manufacture approach of the semiconductor device of the gestalt 1 this operation is explained.

[0032] First, as shown in drawing 3 , two or more semiconductor devices, such as MISFET, form a wiring layer 2 on the principal plane of the semi-conductor substrate 1 which is the semi-conductor wafer formed on the principal plane. Then, an insulator layer 3 is formed on the principal plane of said semi-conductor substrate 1, and opening of the opening 4 which reaches this insulator layer 3 at a wiring layer 2 is carried out. This opening 4 does not need the opening area which can not necessarily be used as a bonding pad in this invention, although usually used also as a bonding pad.

[0033] Next, as shown in drawing 4 , a wiring layer 5 is formed in the front face of the insulator layer 3 also including the interior of opening 4. This wiring layer 5 forms chromium, copper, and chromium by the sputtering method one by one, and forms them by processing this cascade screen by the photolithography technique and etching. Said wiring layer 5 is used in order to rearrange the location of the connection terminal to the exterior in the location of arbitration from opening 4. Moreover, said wiring layer 5 may be formed by depositing chromium or titanium by the sputtering method, considering as the seed film and depositing copper or nickel on the front face of the insulator layer 3 also including the interior of opening 4 with plating continuously.

[0034] Next, as shown in drawing 5 , the surface protective coat 6 is deposited on the principal plane of the semi-conductor substrate 1. Continuously, after carrying out opening of the opening 7 which reaches a wiring layer 5 to the terminal formation location on the principal plane of this surface protective coat 6, the metal post 8 for connecting electrically the solder bump 12 who explains it as a wiring layer 5 later through this opening 7 is formed in it. After this metal post 8 deposits copper with

plating, it is formed by processing it by etching. Moreover, the surface protective coat 6 also has the effectiveness of substrate flattening of the seed film deposited before forming the copper used as the metal post 8 with plating.

[0035] Next, as shown in drawing 6 , width of face forms in the division field 9 on the principal plane of the semi-conductor substrate 1 the slot 10 which is about 100 micrometers by dicing.

[0036] Next, as shown in drawing 7 , the resin 11 for the closures is applied so that the top face of said metal post 8 may be exposed on the principal plane of the semi-conductor substrate 1 including the interior of said slot 10.

[0037] Next, as shown in drawing 8 , the solder bump 12 is connected to the top face which said metal post 8 exposed. This solder bump 12 prints soldering paste for example, with a metal mask, and forms by heating that soldering paste.

[0038] Continuously, the semiconductor device shown in drawing 1 (a) and (b) carries out abbreviation completion by dicing cutting the semi-conductor substrate 1 and the resin 11 for the closures, and dividing them.

[0039] Since, as for the semiconductor device shown with the gestalt 1 of this operation, the resin 11 for the closures has covered the principal plane and side face of the semi-conductor substrate 1, the adhesive strength of the resin 11 for the closures and a semi-conductor substrate becomes strong. Therefore, exfoliation of the resin 11 for the closures and the semi-conductor substrate 1 can be prevented, for example, reinforcement of the metal post 8 for the improvement in the humidity-tolerant reliability of the semi-conductor substrate 1 and connection with the exterior can be performed. That is, after two or more semiconductor chips formed in the semi-conductor wafer through the wafer process are put in block with the condition of a semi-conductor wafer and carry out a resin seal, even if it uses the WPP technique which cuts down each semiconductor device from the semi-conductor wafer, it becomes possible to manufacture a reliable semiconductor device.

[0040] Moreover, since it is the configuration which the semi-conductor substrate 1 exposed to the rear face, and it excels in the heat dissipation effectiveness and the semiconductor device shown with the gestalt 1 of this operation can be attached in said exposed semi-conductor substrate by the direct radiation fin, it can radiate heat effectively.

[0041] (Gestalt 2 of operation) The manufacture approach of the semiconductor device of the gestalt 2 this operation grinds the rear face of the semi-conductor substrate 1 of the semiconductor device shown with the gestalt 1 of said operation, and the resin for the closures deposited on the interior of a slot 10 is exposed at the rear face of the semi-conductor substrate 1 from the base of said slot 10. Other members and processes are the same as the gestalt 1 of said operation. Therefore, the explanation about the same member as them and a process is omitted.

[0042] the sectional view having shown an example of a semiconductor device by which drawing 9 (a) is manufactured according to the gestalt 2 of this operation — it is — (b) — a part of the semiconductor device — it is a fracture perspective view.

[0043] Since rear-face polish of both the semi-conductor substrate 1 and the resin 11 for the closures has been carried out, the semiconductor device manufactured according to the gestalt 2 of this operation has the thin board thickness of said semi-conductor substrate 1, and the description is for said resin 11 for the closures to have covered completely the side face of said semi-conductor substrate 1. Since the board thickness of said semi-conductor substrate 1 is thin, the mechanical property of the semiconductor device shown with the gestalt 2 of this operation becomes closer to the resin for the closures than the mechanical property of the semiconductor device shown with the gestalt 1 of said operation.

[0044] Moreover, drawing 10 is the sectional view showing an example in the condition that the semiconductor device manufactured according to the gestalt 1 of this operation was mounted in the resin printed circuit board 13. The mechanical property of the semiconductor device shown with the

gestalt 2 of this operation Since it is closer to said resin 11 for the closures than the mechanical property of the semiconductor device shown with the gestalt 1 of said operation, Since distortion of the solder bump 12 can be controlled from the semiconductor device shown with the gestalt 1 of said operation even when distortion by the difference of a coefficient of thermal expansion occurs between said semiconductor device and the resin printed circuit board 13 which has the connection pad 14 It can improve rather than the semiconductor device in which the dependability of electrical installation was shown with the gestalt 1 of said operation.

[0045] Next, according to drawing 11 , the manufacture approach of the semiconductor device of the gestalt 2 this operation is explained.

[0046] The process of drawing 3 in the manufacture approach of the semiconductor device the carrying 1 said operation – drawing 7 of the manufacture approach of the semiconductor device of the gestalt 2 this operation is the same.

[0047] Then, as shown in drawing 11 , the rear face of the semi–conductor substrate 1 is ground, and board thickness of the semi–conductor substrate 1 is set to 30 micrometers – about 250 micrometers. At this time, the resin 11 for the closures deposited on the interior of a slot 10 serves as a configuration exposed to the rear face of the semi–conductor substrate 1 from the base of a slot 10.

[0048] Subsequent processes are the same as the process after drawing 8 in the gestalt 1 of said operation.

[0049] In the process in which the quality of the material of a semi–conductor substrate forms a solder bump with a silicon single crystal when the board thickness is 250 micrometers or less, although destruction may arise in a semi–conductor substrate, since the side face of the semi–conductor substrate 1 is completely covered and reinforced by the resin 11 for the closures, the semiconductor device manufactured by the manufacture approach of the gestalt 2 this operation has a strong mechanical strength. Therefore, it becomes possible in the state of the semi–conductor wafer before cutting said semi–conductor substrate 1 in the division field 9 and dividing into each semiconductor chip to form a solder bump, and the productive efficiency of CSP of thin wafer level can be improved.

[0050] Moreover, the sectional view in the condition of having mounted the semiconductor device shown in drawing 12 with the gestalt 2 of two or more operations of these in the resin printed circuit board 13 is shown. Since semiconductor devices 15, 16, 17, and 18 become possible [mounting in the condition of having touched without opening the tooth space between these semiconductor devices since it insulated electrically by the resin 11 for the closures, respectively], they can improve the packaging density of the semiconductor device to said resin printed circuit board 13.

[0051] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of implementation of invention, it cannot be overemphasized that it can change variously in the range which this invention is not restricted to the gestalt of said operation, and does not deviate from the summary.

[0052]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated by this application is explained briefly.

[0053] (1) Since exfoliation of the resin for the closures and a semi–conductor substrate can be prevented, the moisture resistance of a semiconductor device is improved and the reinforcement effectiveness of the post for connection with the exterior can be reinforced.

[0054] (2) The difference of the coefficient of thermal expansion between a semiconductor device and the resin printed circuit board in which this semiconductor device was mounted becomes small, and since distortion produced by the solder bump of the external connection of a semiconductor device is eased, the dependability of the electrical installation of a semiconductor device and a resin substrate can be improved.

[0055] (3) A solder bump can be formed in the state of the semi–conductor wafer before dividing into

each semiconductor chip, without destroying a semi-conductor wafer by mechanical stress, since it is the structure where the semiconductor device was reinforced by the resin for the closures.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] the important section sectional view having shown an example of the semiconductor device with which (a) is manufactured with the gestalt 1 of operation of this invention, and (b) showed an example of the semiconductor device manufactured with the gestalt 1 of operation — it is a fracture perspective view a part.
[Drawing 2] The semiconductor device manufactured with the gestalt 1 of operation is the important section sectional view showing an example in the condition of having been mounted in the resin printed circuit board.
[Drawing 3] It is the important section sectional view having shown an example of the manufacture approach of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process.
[Drawing 4] It is an important section sectional view in the production process of the semiconductor integrated circuit equipment following drawing 3 .
[Drawing 5] It is an important section sectional view in the production process of the semiconductor integrated circuit equipment following drawing 4 .
[Drawing 6] It is an important section sectional view in the production process of the semiconductor integrated circuit equipment following drawing 5 .
[Drawing 7] It is an important section sectional view in the production process of the semiconductor integrated circuit equipment following drawing 6 .
[Drawing 8] It is an important section sectional view in the production process of the semiconductor integrated circuit equipment following drawing 7 .
[Drawing 9] the important section sectional view having shown an example of the semiconductor device with which (a) is manufactured with the gestalt 2 of operation of this invention, and (b) showed an example of the semiconductor device manufactured with the gestalt 2 of operation — it is a fracture perspective view a part.
[Drawing 10] The semiconductor device manufactured with the gestalt 2 of operation is the important section sectional view showing an example in the condition of having been mounted in the resin printed circuit board.
[Drawing 11] It is the important section sectional view having shown an example of the manufacture approach of the semiconductor integrated circuit equipment of the gestalt 2 of operation.
[Drawing 12] The semiconductor device manufactured with the gestalt 2 of two or more operations is the important section sectional view showing an example in the condition of having been mounted in the

resin printed circuit board.

[Description of Notations]

1 Semi-conductor Substrate
2 Wiring Layer
3 Insulator Layer
4 Opening
5 Wiring Layer
6 Surface Protective Coat
7 Opening
8 Metal Post
9 Division Field
10 Slot
11 Resin for Closures
12 Solder Bump
13 Resin Printed Circuit Board
14 Connection Pad
15 Semiconductor Device
16 Semiconductor Device
17 Semiconductor Device
18 Semiconductor Device

[Translation done.]

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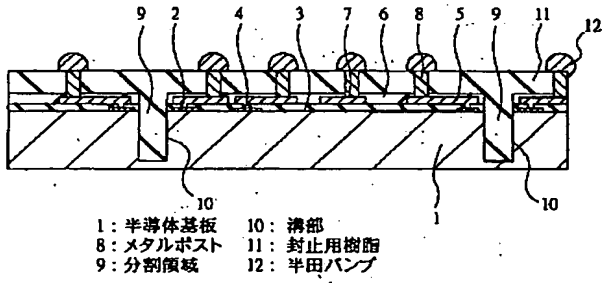
(54)【発明の名称】　半導体装置の製造方法および半導体装置

(57)【要約】
【課題】　半導体装置と樹脂プリント基板との間の歪みを緩和し、半導体装置と樹脂プリント基板との電気的接続の信頼性を向上する。
【解決手段】　溝部10の内部を含む半導体基板1の主面上に封止用樹脂11を塗布し、メタルポスト8の上面に半田バンプ12を形成後、分割領域9に沿って半導体基板1および封止用樹脂11をダイシングにより切断し、半導体基板1の主面および側面が封止用樹脂11で覆われた形状の個々の半導体装置に分割することで、半導体装置と樹脂プリント基板との間の熱膨張係数の差を小さくする。

図 8



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【特許請求の範囲】

【請求項１】　（ａ）分割領域によって区画された複数のチップ形成領域を有する半導体ウエハであって、前記複数のチップ形成領域の各々が複数の半導体素子と複数のボンディングパッドとを有する半導体ウエハを準備する工程、（ｂ）前記チップ形成領域の各々の複数のボンディングパッドに電気的に接続された導体部を形成する工程、（ｃ）前記分割領域に溝部を形成する工程、（ｄ）前記溝部内を含む前記半導体ウェハの主面上に封止用絶縁膜を形成する工程、（ｅ）前記半導体ウエハを前記溝部に沿って切断することにより、前記導体部が形成され、前記封止用絶縁膜の一部が側面に形成された複数の半導体チップを形成する工程、を含むことを特徴とする半導体装置の製造方法。

【請求項２】　（ａ）分割領域によって区画された複数のチップ形成領域を有する半導体ウエハであって、前記複数のチップ形成領域の各々が複数の半導体素子と複数のボンディングパッドとを有する半導体ウエハを準備する工程、（ｂ）前記チップ形成領域の各々の複数のボンディングパッドに電気的に接続された導体部を形成する工程、（ｃ）前記分割領域に溝部を形成する工程、（ｄ）前記溝部内を含む前記半導体ウェハの主面上に封止用絶縁膜を形成する工程、（ｅ）前記半導体ウエハの裏面を研磨し、前記溝部内に形成した封止用絶縁膜を前記溝部の底面から前記半導体ウェハの裏面に露出させる工程、（ｆ）前記半導体ウエハを前記溝部に沿って切断することにより、前記導体部が形成され、前記封止用絶縁膜の一部が側面に形成された複数の半導体チップを形成する工程、を含むことを特徴とする半導体装置の製造方法。

【請求項３】　請求項１または２記載の半導体装置の製造方法であって、前記複数の半導体チップを形成する前に前記半導体ウェハの主面上の端子位置に半田バンプを電気的に接続する工程を含むことを特徴とする半導体装置の製造方法。

【請求項４】　半導体チップの主面上に複数の半導体素子が形成された半導体装置であって、前記半導体チップの上面および側面が封止用絶縁膜で覆われ、下面には前記半導体チップの底面が露出する構造を有することを特徴とする半導体装置。

【請求項５】　請求項４記載の半導体装置であって、前記半導体チップの側面の一部または全面が封止用絶縁膜で覆われた構造を有することを特徴とする半導体装置。

【請求項６】　請求項４または５に記載の半導体装置であって、前記半導体チップは封止用絶縁膜で覆われた後、下面が研磨された構造を有することを特徴とする半導体装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体装置の製造

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方法および半導体装置技術に関し、特に、半導体装置のパッケージング技術に適用して有効な技術に関するものである。

【０００２】

【従来の技術】電子機器の小型・軽量化に伴い、半導体装置のパッケージについても薄型化や小型・軽量化が求められている。ＣＳＰ（Chip Size Package ）は、半導体チップのサイズと同等またはわずかに大きいパッケージの総称であり、小型・軽量化を実現できる上、内部の配線長を短くすることができるので、信号遅延や雑音等を低減できるパッケージ構造として実用化されている。ＣＳＰの製造方法は、種々あるが、半導体ウエハから半導体チップを切り出した後、その半導体チップを、半導体チップと同等またはわずかに大きな配線基板上に搭載し、その状態で樹脂封止するのが一般的である。

【０００３】一方、このようなＣＳＰの他の製造技術として、ウエハプロセスパッケージ（Wafer Process Package ；以下、ＷＰＰと略す）技術がある。この技術は、ウエハプロセスを経て半導体ウエハに形成された複数の半導体チップを、半導体ウエハの状態のまま一括して樹脂封止した後、その半導体ウエハから個々の半導体装置を切り出す技術である。この技術においては、製造工程を簡略化でき、製造コストを低減でき、さらに、ＣＳＰを大幅に小型化することができるという優れた特徴がある。

【０００４】なお、この種の技術については、例えば日経ＢＰ社、１９９９年２月１日発行、「日経マイクロデバイス１９９９年２月号」ｐ５６に記載があり、ウエハプロセスにおいてパッケージの組立を行うＣＳＰの製造技術が開示されており、半導体ウエハから個々の半導体装置が切り出された状態では、その断面は半導体チップの主面上に封止用樹脂が重なった構造になっている。

【０００５】

【発明が解決しようとする課題】しかし、このＷＰＰにおいては、半導体ウエハの複数の半導体チップを一括して樹脂封止した後、その半導体ウエハから個々の半導体チップを切り出すので、半導体チップの側面および裏面は樹脂封止されない。このため、半導体装置の耐湿性や遮光性等のようなパッケージ特性の向上が阻害される課題がある。また、半導体チップの主面上に封止用樹脂が重なっているだけの構造のため、前記半導体チップと前記封止用樹脂との接着性が悪くなり、前記半導体チップの湾曲などにより剥離する場合があり、前記半導体チップの外部への半田接続部の破壊が発生したり、樹脂封止の信頼性が低下したりする。

【０００６】さらに、このＷＰＰにおいては、半導体チップに比べて封止用樹脂の膜厚が薄いため、半導体装置の機械的性質は半導体チップに依存することになる。そのため、前記半導体装置の外部のガラスエポキシ等の樹脂製の基板と前記半導体装置との熱膨張係数の差に起因

する歪みが緩和できないため、前記半導体装置の外部接続部の半田の機械的信頼度が低下する。

【０００７】本発明の目的は、半導体装置のパッケージの耐湿信頼性および外部への接続用ポストの補強効果を向上させることができる技術を提供することにある。

【０００８】また、本発明の他の目的は、前記半導体装置と外部基板との電気的接続性を向上させる技術を提供することにある。

【０００９】本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

【００１０】

【課題を解決するための手段】本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、次のとおりである。

【００１１】（１）本発明の半導体装置は、ウエハプロセスを経て半導体ウエハに形成された複数の半導体チップを、半導体ウエハの状態のまま一括して樹脂封止した後、その半導体ウエハから切り出された半導体装置であって、半導体基板の側面の一部または全面を封止用樹脂で被覆したものである。

【００１２】（２）本発明の半導体装置は、半導体基板の主面に半導体素子が形成され、その主面および前記半導体基板の側面を封止用樹脂で被覆し、裏面は半導体基板が露出したものである。

【００１３】（３）本発明の半導体装置は、半導体基板の主面および前記半導体基板の側面を封止用樹脂で被覆した後、前記半導体基板の裏面を研磨し、前記半導体基板の側面の全面を樹脂封止した形状となるものである。

【００１４】（４）本発明の半導体装置の製造方法は、以下の工程を含んでいる。

【００１５】（ａ）分割領域によって区画された複数のチップ形成領域を有する半導体ウエハであって、前記複数のチップ形成領域の各々が複数の半導体素子と複数のボンディングパッドとを有する半導体ウエハを準備する工程、（ｂ）前記チップ形成領域の各々の複数のボンディングパッドに電気的に接続された導体部を形成する工程、（ｃ）前記分割領域に溝部を形成する工程、（ｄ）前記溝部内を含む前記半導体ウェハの主面上に封止用絶縁膜を形成する工程、（ｅ）前記半導体ウエハを前記溝部に沿って切断することにより、前記導体部が形成され、前記封止用絶縁膜の一部が側面に形成された複数の半導体チップを形成する工程。

【００１６】（５）本発明の半導体装置の製造方法は、以下の工程を含んでいる。

【００１７】（ａ）分割領域によって区画された複数のチップ形成領域を有する半導体ウエハであって、前記複数のチップ形成領域の各々が複数の半導体素子と複数のボンディングパッドとを有する半導体ウエハを準備する工程、（ｂ）前記チップ形成領域の各々の複数のボンディングパッドに電気的に接続された導体部を形成する工程、（ｃ）前記分割領域に溝部を形成する工程、（ｄ）前記溝部内を含む前記半導体ウェハの主面上に封止用絶縁膜を形成する工程、（ｅ）前記半導体ウエハの裏面を研磨し、前記溝部内に形成した封止用絶縁膜を前記溝部の底面から前記半導体ウェハの裏面に露出させる工程、（ｆ）前記半導体ウエハを前記溝部に沿って切断することにより、前記導体部が形成され、前記封止用絶縁膜の一部が側面に形成された複数の半導体チップを形成する工程。

【００１８】上記（４）、（５）の工程によれば、封止用樹脂が半導体基板の主面および側面を覆うため、封止用樹脂と半導体基板の接着力が強くなる。そのため、封止用樹脂と半導体基板の剥離が防止でき、たとえば半導体基板の耐湿信頼性の向上、および外部との接続用のポストの補強ができる。

【００１９】さらに、前記外部との接続用のポストは、半導体基板との接着がよい封止用樹脂で保持されており、半導体装置の機械的性質は前記封止用樹脂に近いため、前記半導体装置と前記半導体装置が実装される樹脂プリント基板との間に熱膨張係数の差による歪みを緩和し、電気的接続の信頼性が向上できる。

【００２０】また、（５）の工程によれば、半導体基板の側面が完全に封止用樹脂で覆われ、補強されているので、半導体装置の機械的強度が強くなる。そのため、前記半導体基板を切断して、個々の半導体チップに分割する前の、半導体ウェハの状態で、半田バンプを形成することが可能となり、薄型ウェハ・レベルのＣＳＰの生産効率を向上することができる。

【００２１】

【発明の実施の形態】以下、本発明の実施の形態を図面に基づいて詳細に説明する。なお、実施の形態を説明するための全図において、同一の機能を有する部材には同一の符号を付し、その繰り返しの説明は省略する。

【００２２】（実施の形態１）本実施の形態１においては、本発明を、たとえば携帯電話、携帯型パーソナルコンピュータまたは携帯型の情報処理装置等のような小型・携帯型の電子装置が有するＤＲＡＭ（Dynamic Random Access Memory）、ＳＲＡＭ（Static RandomAccess Memory）、またはマイクロコンピュータに用いるＣＳＰ型の半導体装置の製造方法に適用した場合について説明する。

【００２３】図１（ａ）は、本実施の形態１により製造される半導体装置の一例を示した断面図であり、（ｂ）はその半導体装置の一部破断斜視図である。

【００２４】半導体基板１は、たとえばシリコン単結晶からなり、その主面上に、たとえばＭＩＳＦＥＴ（Metal Insulator Semiconductor Field Effect Transistor）等のような複数の半導体素子および複数の配線層２が形成された半導体ウェハを、分割領域にて切断するこ

とで形成した半導体チップである。

【００２５】配線層２は、たとえばアルミニウム、アルミニウム－銅合金またはアルミニウム－シリコン－銅合金等からなる。この配線層２は、絶縁膜３で保護されている。

【００２６】絶縁膜３は、たとえばポリイミドなどの有機膜、窒化シリコン膜、または酸化シリコン膜からなる。前記絶縁膜３には、開口部４が形成されており、この開口部４を通じて、配線層２と絶縁膜３の上面に形成された配線層５とは互いに電気的に接続されている。配線層５は、たとえば銅または銅合金等からなる。

【００２７】配線層５は、ボンディングパッドの再配置用の配線であり、外部との接続端子位置をメタルポスト８にするために用いられる。この配線層５の表面は、たとえばポリイミドなどの有機膜からなる表面保護膜６によって被覆されている。この場合、たとえばα線の阻止能力を向上させることが可能となる。

【００２８】表面保護膜６の一部には、配線層５の一部が露出するような開口部７が形成され、この開口部７から露出する配線部分がボンディングパッドを形成する。このボンディングパッドは、前記半導体チップに形成された前記半導体素子や回路等の電極を外部に引き出す電極である。また、このボンディングパッドには、メタルポスト８を介して半田バンプ１２が電気的に接続されている。メタルポスト８は、たとえば銅からなる。半田バンプ１２は、たとえば金または鉛－錫合金半田からなる。

【００２９】封止用樹脂（封止用絶縁膜）１１は、前記半導体基板１の側壁部も覆っており、半導体基板１との食い付きアンカー効果により、前記半導体基板１との接着性に優れる。このため、前記半導体基板１および配線層２の耐湿信頼性が向上するとともに、メタルポスト８の補強効果が増す。この封止用樹脂１１は、エポキシ系の樹脂からなる。

【００３０】図２は、本実施の形態１により製造される半導体装置が樹脂プリント基板１３に実装された状態の一例を示す断面図である。メタルポスト８は、半導体基板１との接着がよい封止用樹脂１１で保持されており、前記半導体装置の機械的性質は前記封止用樹脂１１に近いため、前記半導体装置と接続パッド１４を有する樹脂プリント基板１３との間に熱膨張係数の差による歪みが発生した場合でも、半田バンプ１２の歪みを抑制できるので、電気的接続の信頼性が向上できる。

【００３１】次に、図３～図８に従って、本実施の形態１の半導体装置の製造方法について説明する。

【００３２】まず、図３に示すように、たとえばＭＩＳＦＥＴ等のような複数の半導体素子が主面上に形成された半導体ウェハである半導体基板１の主面上に、配線層２を形成する。続いて、前記半導体基板１の主面上に絶縁膜３を形成し、この絶縁膜３に配線層２に達する開口部４を開口する。この開口部４は、通常はボンディングパッドとしても用いられるが、本発明においては必ずしもボンディングパッドとして用いることが可能な開口面積は必要としない。

【００３３】次に、図４に示すように、開口部４の内部も含む絶縁膜３の表面に配線層５を形成する。この配線層５は、クロム、銅、クロムを順次スパッタリング法にて成膜し、この積層膜をフォトリソグラフィー技術およびエッチングにより加工することで形成する。前記配線層５は、外部への接続端子の位置を開口部４から任意の位置に再配置するために用いられる。また、前記配線層５は、開口部４の内部も含む絶縁膜３の表面に、たとえばクロムまたはチタンなどをスパッタリング法で堆積し、シード膜とし、続けて、銅またはニッケルなどをメッキ法にて堆積することで形成してもよい。

【００３４】次に、図５に示すように、半導体基板１の主面上に表面保護膜６を堆積する。続けて、この表面保護膜６の主面上の端子形成位置に、配線層５に達する開口部７を開口した後、配線層５と後で説明する半田バンプ１２とを、この開口部７を通じて電気的に接続するためのメタルポスト８を形成する。このメタルポスト８は、たとえば、メッキ法により銅を堆積した後、エッチングにより加工することで形成する。また、表面保護膜６は、メタルポスト８となる銅をメッキ法により形成する前に堆積されるシード膜の下地平坦化の効果も有する。

【００３５】次に、図６に示すように、半導体基板１の主面上の分割領域９にダイシングにより、たとえば幅が１００μｍ程度の溝部１０を形成する。

【００３６】次に、図７に示すように、前記溝部１０の内部を含む半導体基板１の主面上に、前記メタルポスト８の上面が露出するように封止用樹脂１１を塗布する。

【００３７】次に、図８に示すように、前記メタルポスト８の露出した上面に半田バンプ１２を接続する。この半田バンプ１２は、たとえばメタルマスクにより半田ペーストを印刷し、その半田ペーストを加熱することにより形成する。

【００３８】続けて、半導体基板１および封止用樹脂１１をダイシングにより切断し、分割することで、図１（ａ）および（ｂ）に示す半導体装置が略完成する。

【００３９】本実施の形態１で示した半導体装置は、封止用樹脂１１が半導体基板１の主面および側面を覆っているため、封止用樹脂１１と半導体基板の接着力が強くなる。そのため、封止用樹脂１１と半導体基板１の剥離が防止でき、たとえば半導体基板１の耐湿信頼性の向上、および外部との接続のためのメタルポスト８の補強ができる。すなわち、ウエハプロセスを経て半導体ウエハに形成された複数の半導体チップを、半導体ウエハの状態のまま一括して樹脂封止した後、その半導体ウエハから個々の半導体装置を切り出すＷＰＰ技術を用いても、信頼性の高い半導体装置を製造することが可能にな

る。

【００４０】また、本実施の形態１で示した半導体装置は、その裏面に半導体基板１が露出した形状なので、放熱効果にすぐれ、前記露出した半導体基板に直接放熱フィンが取り付けることが可能なので、効果的に放熱を行うことができる。

【００４１】（実施の形態２）本実施の形態２の半導体装置の製造方法は、前記実施の形態１で示した半導体装置の半導体基板１の裏面を研磨し、溝部１０の内部に堆積した封止用樹脂を前記溝部１０の底面から半導体基板１の裏面へ露出させたものである。その他の部材および工程は、前記実施の形態１と同様である。したがって、それら同様の部材および工程についての説明は省略する。

【００４２】図９（ａ）は、本実施の形態２により製造される半導体装置の一例を示した断面図であり、（ｂ）はその半導体装置の一部破断斜視図である。

【００４３】半導体基板１および封止用樹脂１１はともに裏面研磨してあるため、本実施の形態２により製造される半導体装置は、前記半導体基板１の板厚が薄く、前記封止用樹脂１１が前記半導体基板１の側面を完全に覆っていることに特徴がある。前記半導体基板１の板厚が薄いため、本実施の形態２で示す半導体装置の機械的性質は、前記実施の形態１で示した半導体装置の機械的性質よりも封止用樹脂に近くなる。

【００４４】また、図１０は、本実施の形態１により製造される半導体装置が樹脂プリント基板１３に実装された状態の一例を示す断面図である。本実施の形態２で示す半導体装置の機械的性質は、前記実施の形態１で示した半導体装置の機械的性質よりも前記封止用樹脂１１に近いため、前記半導体装置と接続パッド１４を有する樹脂プリント基板１３との間に熱膨張係数の差による歪みが発生した場合でも、前記実施の形態１で示した半導体装置より半田バンプ１２の歪みを抑制できるので、電気的接続の信頼性を前記実施の形態１で示した半導体装置よりも向上することができる。

【００４５】次に、図１１に従って、本実施の形態２の半導体装置の製造方法について説明する。

【００４６】本実施の形態２の半導体装置の製造方法は、前記実施の携帯１の半導体装置の製造方法における図３～図７の工程までは同様である。

【００４７】その後、図１１に示すように、半導体基板１の裏面を研磨し、その半導体基板１の板厚を、たとえば３０μｍ～２５０μｍ程度とする。このとき、溝部１０の内部に堆積した封止用樹脂１１が、溝部10の底面から半導体基板１の裏面へ露出した形状となる。

【００４８】以降の工程は、前記実施の形態１における図８以降の工程と同様である。

【００４９】半導体基板の材質が、たとえばシリコン単結晶で、その板厚が２５０μｍ以下の場合、半田バンプを形成する工程において、半導体基板に破壊が生じる場合があるが、本実施の形態２の製造方法にて製造される半導体装置は、半導体基板１の側面が完全に封止用樹脂１１で覆われ、補強されているので、機械的強度が強い。そのため、前記半導体基板１を分割領域９にて切断して、個々の半導体チップに分割する前の、半導体ウェハの状態で、半田バンプを形成することが可能となり、薄型ウェハ・レベルのＣＳＰの生産効率を向上することができる。

【００５０】また、図１２に、複数の本実施の形態２で示した半導体装置を樹脂プリント基板１３に実装した状態の断面図を示す。半導体装置１５、１６、１７および１８は、それぞれ封止用樹脂11で電気的に絶縁されているので、それら半導体装置間のスペースをあけずに接した状態で実装することが可能となるので、前記樹脂プリント基板１３への半導体装置の実装密度を向上することができる。

【００５１】以上、本発明者によってなされた発明を発明の実施の形態に基づいて具体的に説明したが、本発明は前記実施の形態に限られるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。

【００５２】

【発明の効果】本願によって開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば以下の通りである。

【００５３】（１）封止用樹脂と半導体基板の剥離が防止できるため、半導体装置の耐湿性を向上し、外部への接続用のポストの補強効果を増強できる。

【００５４】（２）半導体装置と、この半導体装置が実装された樹脂プリント基板との間の熱膨張係数の差が小さくなり、半導体装置の外部接続部の半田バンプに生じる歪みを緩和するので、半導体装置と樹脂基板の電気的接続の信頼性を向上できる。

【００５５】（３）半導体装置が封止用樹脂で補強された構造なので、半導体ウェハを機械的ストレスで破壊することなく、個々の半導体チップに分割する前の半導体ウェハの状態で半田バンプを形成することができる。

【図面の簡単な説明】

【図１】（ａ）は本発明の実施の形態１で製造される半導体装置の一例を示した要部断面図、（ｂ）は実施の形態１で製造される半導体装置の一例を示した一部破断斜視図である。

【図２】実施の形態１で製造される半導体装置が樹脂プリント基板に実装された状態の一例を示す要部断面図である。

【図３】実施の形態１の半導体集積回路装置の製造方法の一例をその工程順に示した要部断面図である。

【図４】図３に続く半導体集積回路装置の製造工程中の要部断面図である。

【図５】図４に続く半導体集積回路装置の製造工程中の要部断面図である。

【図６】図５に続く半導体集積回路装置の製造工程中の要部断面図である。

【図７】図６に続く半導体集積回路装置の製造工程中の要部断面図である。

【図８】図７に続く半導体集積回路装置の製造工程中の要部断面図である。

【図９】（ａ）は本発明の実施の形態２で製造される半導体装置の一例を示した要部断面図、（ｂ）は実施の形態２で製造される半導体装置の一例を示した一部破断斜視図である。

【図１０】実施の形態２で製造される半導体装置が樹脂プリント基板に実装された状態の一例を示す要部断面図である。

【図１１】実施の形態２の半導体集積回路装置の製造方法の一例を示した要部断面図である。

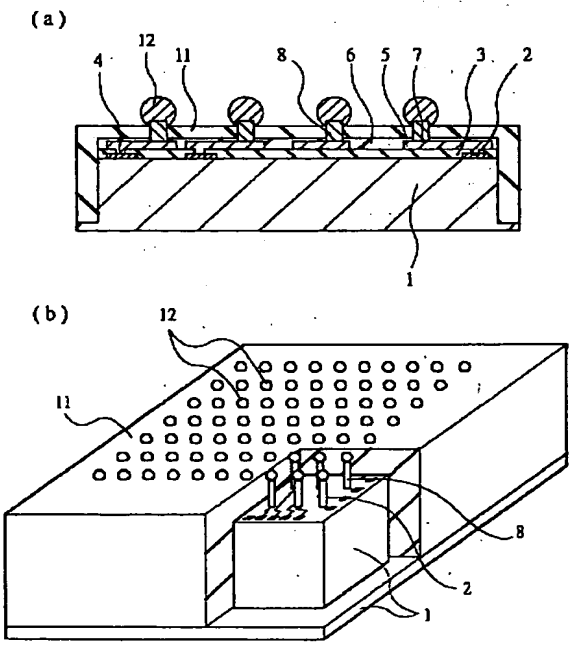
【図１２】複数個の実施の形態２で製造される半導体装置が樹脂プリント基板に実装された状態の一例を示す要部断面図である。

【符号の説明】

１　半導体基板
２　配線層
３　絶縁膜
４　開口部
５　配線層
６　表面保護膜
７　開口部
８　メタルポスト
９　分割領域
１０　溝部
１１　封止用樹脂
１２　半田バンプ
１３　樹脂プリント基板
１４　接続パッド
１５　半導体装置
１６　半導体装置
１７　半導体装置
１８　半導体装置

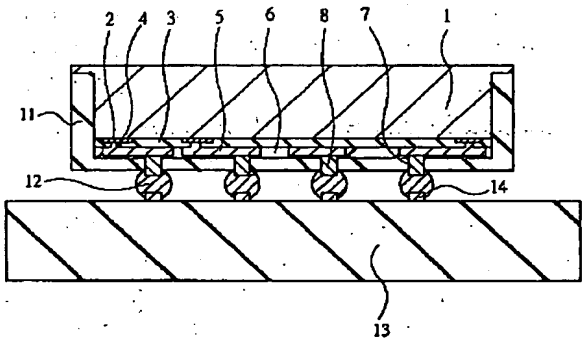
【図１】

図 1



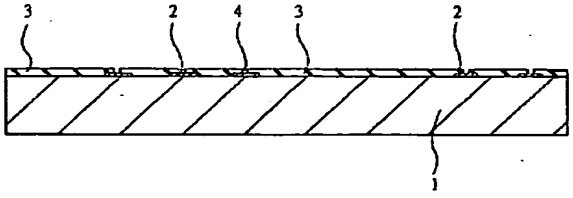
【図２】

図 2



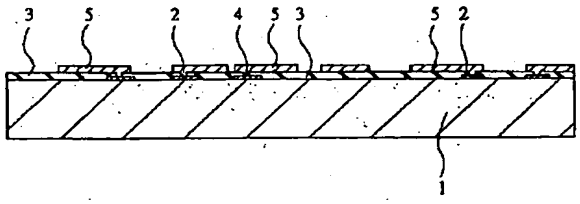
【図３】

図 3



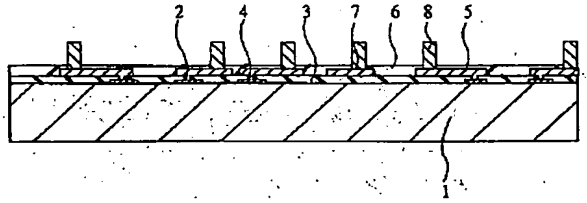
【図４】

図 4



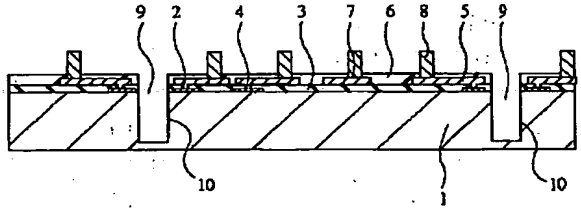
【図５】

図 5



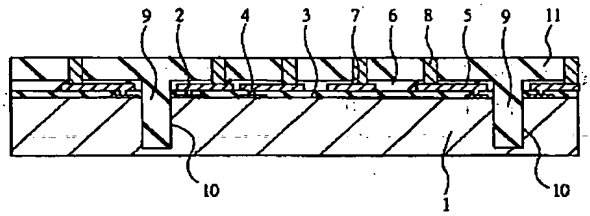
【図６】

図 6



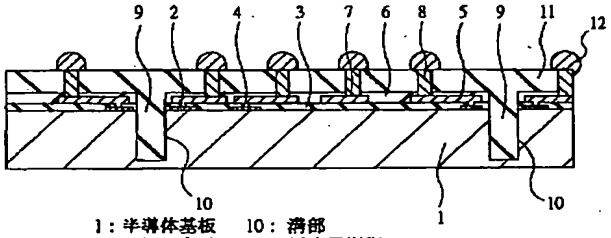
【図７】

図 7



【図８】

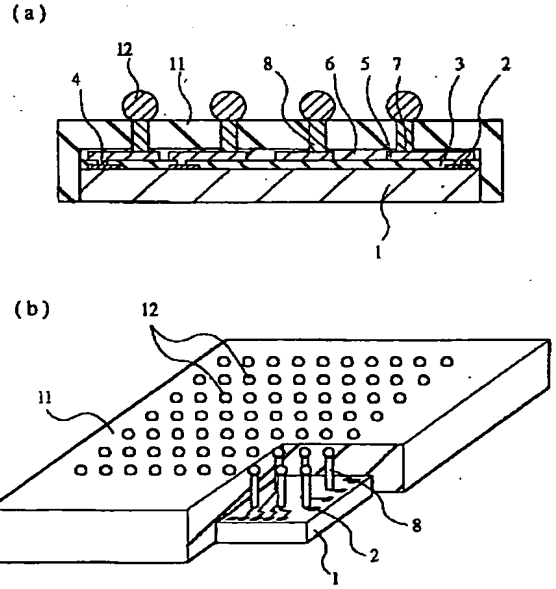
図 8



1：半導体基板　10：溝部
8：メタルポスト　11：封止用樹脂
9：分割領域　12：半田バンプ

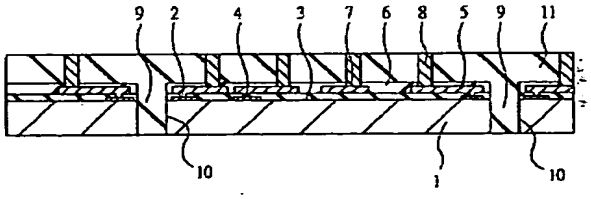
【図９】

図 9



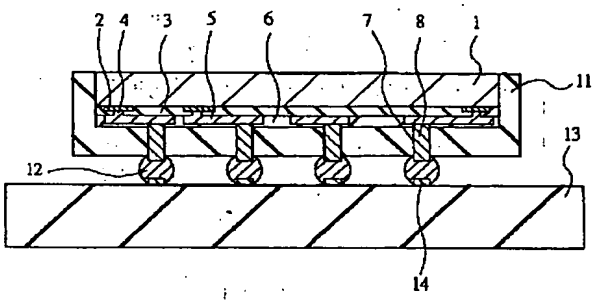
【図１１】

図 11



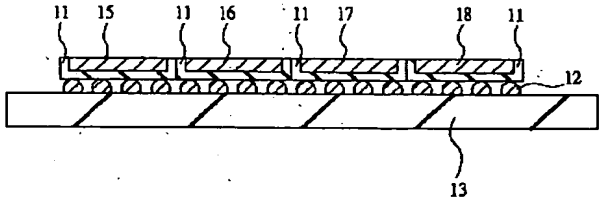
【図１０】

図 10



【図１２】

図 12



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	23/29			604B
	23/31			604S
				604E
			23/30	D

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